REMARKS/ARGUMENTS

Pending claims 1, 3-4, 9, 18, 20-21 stand rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 5,812,817 (Hovis) in view of U.S. Patent No. 6,601,151 (Harris). Applicant respectfully traverses the rejection and respectfully requests reconsideration of the same. As to claim 1, the Office Action contends that Hovis teaches a compression cache that is organized as a sectored cache that has associated tags that are on-die. As support, the Office Action refers to FIG. 1 and column 2, lines 35-37, contending that the sectored cache is taught as segments of memory that are stored in the compression cache. However, Hovis fails to teach or suggest both an organization of a compression cache as a sectored cache or where associated tags are on-die. As to the uncompressed cache 12 of Hovis, all that is taught is that this is a segment of a conventional computer memory, and that "the most active segments of memory" are maintained within uncompressed cache 12. None of this however anywhere teaches or suggests that the cache be organized as a sectored cache. Still further, Hovis nowhere teaches or suggests that the compression cache has associated tags that are on-die. In this regard, the Office Action does not appear to cite anything for such a teaching, as certainly neither column 2, lines 35-37 or 50-51 anywhere teach or suggest this subject matter.

Further regarding claim 1, there is no teaching or suggestion in Hovis that a tag match performed between a memory access request and these on-die associated tags cause a hit signal to be sent to a memory controller to schedule an uncompressed data access. That is, while Hovis teaches that an uncompressed cache directory 18 can be used to access uncompressed cache 12, there is no teaching or suggestion of a tag match that is performed as set forth in claim 1. Still further, there is no teaching or suggestion that this tag match causes a hit signal that schedules an uncompressed data access scheduled by a memory controller. In this regard, Hovis fails to teach or suggest anything with regard to scheduling of an uncompressed data access, and certainly fails to teach or suggest such subject matter as performed by a memory controller coupled to a main memory.

Still further as to claim 1, the Office Action concedes that Hovis fails to teach assigning a higher priority to compressed memory read operations in comparison to other operations. Instead, the Office Action purports to rely on Harris for such a teaching. However, Harris teaches nothing with regard to compressed memory or compressed memory read operations. Instead, Harris simply teaches that read requests for a memory management unit (MMU) given

priority over read requests to a load store unit. Such teaching, however has no bearing on the recited claimed subject matter of assigning of a higher priority to compressed memory read operations in comparison to other read operations. In this regard, the Office Action contends that the suggestion for such teaching is that "processor performance can be enhanced by ascribing memory read requests higher priority than other requests...." Office Action, p. 4. However, all that the recited portion of Harris teaches is that MMU table memory read requests are ascribed a higher source priority level than general memory read requests. This disclosure from Harris simply has no bearing on the recited subject matter of the compressed memory and priority of compressed memory read operations. Accordingly, claim 1 and the claims depending therefrom are patentable over the cited art. For at least the same reasons independent claim 18 and its dependent claims are similarly patentable.

Regarding dependent claim 3, the Office Action contends that setup table 14 is the recited plurality of associated tags incorporated within a memory interface. Applicant respectfully disagrees. Instead, all that setup table 14 is is a directory in memory for the compressed data in the compressed storage 16. Thus Hovis teaches the opposite of that in claim 3. For similar reasons discussed above regarding claims 1 and 3, dependent claim 20 is further patentable.

Pending claims 14, 16-17, 22-23 and 25-29 stand rejected under 35 U.S.C. § 103(a) over Hovis in view of U.S. Patent No. 6,202,126 (Van Doren). Applicant respectfully traverses the rejection. As to independent claim 14, again the Office Action contends that Hovis teaches the recited accessing of uncompressed data responsive to an uncompressed access scheduling by a memory controller if a tag match performed in a memory interface results in a hit. As discussed above regarding claim 1, Hovis fails to teach this scheduling by a memory controller.

The Office Action then concedes that Hovis fails to teach the operations performed on a miss, namely accessing uncompressed data directly from a victim buffer of a memory interface. Instead, the Office Action purports to rely on Van Doren. However Van Doren nowhere teaches or suggests a victim buffer that is of a memory interface coupled to a main memory. Instead, the teaching in Van Doren is that a CPU may include victim buffers for temporary data storage. However, this nowhere teaches or suggests location of the victim buffer in a memory interface, and it certainly nowhere teaches or suggests the storage of uncompressed data from a compression cache of a main memory in such a victim buffer. Instead, in Van Doren the victim buffer is to store data that is evicted from a cache of a CPU. Van Doren, 8:28-40. Simply put,

the motivation contended by the Office Action (*see* Office Action, p. 7) nowhere teaches or suggests the recited victim buffer of a memory interface to store compressed data evicted from a compression memory that is itself of a main memory.

Independent claim 22 is patentable for at least the same reasons discussed above regarding the other independent claims, as both Hovis and Van Doren fail to teach at least the recited memory controller that schedules the uncompressed data access, the victim buffer, an offset calculator, and a second cache to store most recently used pointers. Other than the victim buffer, the Office Action contends that Hovis teaches all of this subject matter. However, the only support is column 3 lines 23-57, which simply teaches a setup table in main memory, and has nothing to do with any of the above recited subject matter. Note that the recited second cache that stores pointers is recited to be in a memory interface. This is not taught or suggested by Hovis. Further as discussed above, Van Doren nowhere teaches a victim buffer to store an entry evicted from a compression cache of a main memory, and certainly not such a victim buffer that is present in a memory interface.

As to claim 23, the Office Action contends that item 10 of FIG. 4 of Hovis is part of a chipset. However, Hovis instead teaches that memory 10 is a conventional computer memory, and nothing teaches the recited chipset of claim 23.

As to dependent claim 25, Hovis nowhere teaches the recited first-in-first-out eviction protocol. Instead, Hovis teaches a least recently used eviction method. As this protocol is not a first-in-first-out protocol, the rejection of claim 25 is further overcome.

Independent claim 26 and its dependent claims are patentable for at least the same reasons discussed above regarding claim 22.

Dependent claims 5-8 and 10-13 standing rejected under 35 U.S.C. §103(a) over Hovis in view of Harris and in further view of Van Doren are overcome for at least the same reasons discussed above regarding the independent claims.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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